Amendments of the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An electric or electronic circuit arrangement (100) comprising at least one layered carrier substrate (10) of a semiconducting or insulating material, at least one integrated circuit constituted by at least two spaced conductor tracks (20, 25) on the carrier substrate (10), at least one dielectric shielding layer (30; 35) situated between the conductor tracks (20, 25) and/or laterally with respect to the conductor tracks (20, 25) and/or on the conductor tracks (20, 25), provided for protecting the integrated circuit from external influences so that the integrated circuit has a specific capacitance (C) determined by the dielectric shielding layer (30; 35), characterized in that at least one signal-generating unit (40) is connected to the contact terminals (22, 27) of the integrated circuit, an output frequency ($f_{meas.}$) of which unit is substantially determined by the specific capacitance (C), in that the signal-generating unit (40) precedes an evaluation unit which includes at least a first counting unit (50) which is clocked at the output frequency ($f_{meas.}$) of the signal-generating unit (40) and in which an actual value count can be determined after a predetermined temporal counting period, at least a second counting unit (55) clocked at a reference frequency (f_{ref}), in which a nominal value count can be determined after the predetermined temporal counting period, and at least one comparator unit (60) for comparing the actual value count with the nominal value count, wherein the signal-generating unit (40) and the evaluation unit (70) are integral parts of the integrated circuit.

2. (Original) A circuit arrangement (100) as claimed in claim 1, characterized in that the conductor tracks (20, 25) are at least sectionally arranged parallel to each other and/or in a meandering intermeshing configuration.

3. (Previously Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that the mutual distance (d) between the conductor tracks (20, 25) is in the micrometer range.

4. (Previously Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that the material of the dielectric shielding layer (30; 35) is epoxy resin or silicon nitrite ($SiNO_2$) or silicon dioxide (SiO_2) or consists of other insulating layers used in the manufacture of semiconductors.

5. (Previously Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that the material of the dielectric shielding layer (30; 35) is also opaque.

6. (Previously Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that the signal-generating unit (40) comprises at least one oscillator circuit consisting of at least one capacitive unit and at least one resistive unit and/or at least one oscillator circuit consisting of at least one capacitive unit and at least one inductive unit.

7. (Previously Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that the evaluation unit (70) is a differential evaluation unit.

8. (Original) A circuit arrangement (100) as claimed in claim 7, characterized in that the evaluation unit (70) is implemented to detect a change of the specific capacitance (C) caused by an at least partial removal of the dielectric shielding layer (30; 35).

9. (Previously Amended) A circuit arrangement (100) a claimed in claim 7, characterized in that the evaluation unit (70) generates the error indication when the actual value deviates from the nominal range.

10. (Previously Amended) A circuit arrangement (100) as claimed in claim 1, characterized in that the first counting unit (50) and/or the second counting unit (55) are/is formed on a digital basis.

11. (Previously Amended) A card comprising at least an electric or electronic circuit arrangement (100) as claimed in claim 1.

12. (Currently Amended) A method of protecting an electric or electronic circuit arrangement (100) of a semiconductor card formed in accordance with the precharacterizing part of claim 1, from manipulation and/or abuse, characterized in that an output frequency ($f_{meas.}$) determined by a specific capacitance (C) is generated in at least one signal-generating unit (40) and provided to an evaluation unit (70) which includes at least a first counting unit (50), at least a second counting unit (55) and at least a comparator unit (60), in that an actual value count is determined after a predetermined temporal counting period in the first counting unit (50) clocked at the output frequency ($f_{meas.}$) of the signal-generating unit (40), in that a nominal value count is determined after the predetermined temporal counting period in the second counting unit (55) clocked at a reference frequency (f_{ref}), in that the actual value count is compared with the nominal value count in the comparator unit (60), wherein the signal-generating unit (40) and the evaluation unit (70) are provided as integral parts of the ~~semiconductor card~~integrated circuit.

13. (Previously Amended) A method as claimed in claim 12, characterized in that the evaluation unit (70) operates on a differential basis.

14. (Original) A method as claimed in claim 13, characterized in that a change of the specific capacitance (C) caused by an at least partial removal of the dielectric shielding layer (30; 35) is detected in the evaluation unit (70).

15. (Previously Amended) A method as claimed in claim 13, characterized in that the error indication is generated in the evaluation unit (70) when the actual value deviates from the nominal range.

16. (Previously Presented) A circuit arrangement as claimed in claim 1, characterized in that the conductor tracks (20, 25) are lithographically applied.

17. (Previously Presented) A circuit arrangement as claimed in claim 1,characterized in that the dielectric shielding layer (30) comprises an insulation layer or passivation layer (30) and/or a protection layer (35).

18. (Previously Presented) A circuit arrangement as claimed in claim 1, characterized in that the specific capacitance (C0 is a lateral and/or parasitic capacitance.

19. (Previously Presented) A circuit arrangement as claimed in claim 1, characterized in that functions of the integrated circuit can be blocked and/or locked and/or interrupted temporarily or permanently in the case of an error indication which occurs when the actual value count is compared with the nominal value count.

20. (Previously Presented) A circuit arrangement (100) as claimed in claim 6, characterized in that the capacitive unit is a capacitor, and the resistive unit is a resistor, and the inductive unit is a coil.

21. (Previously Presented) A method as claimed in claim 12, characterized in that functions of the integrated circuit are blocked and/or locked and/or interrupted temporarily or permanently in the case of an error indication which occurs when the actual value count is compared with the nominal value.